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Bibliography.

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## Summary.

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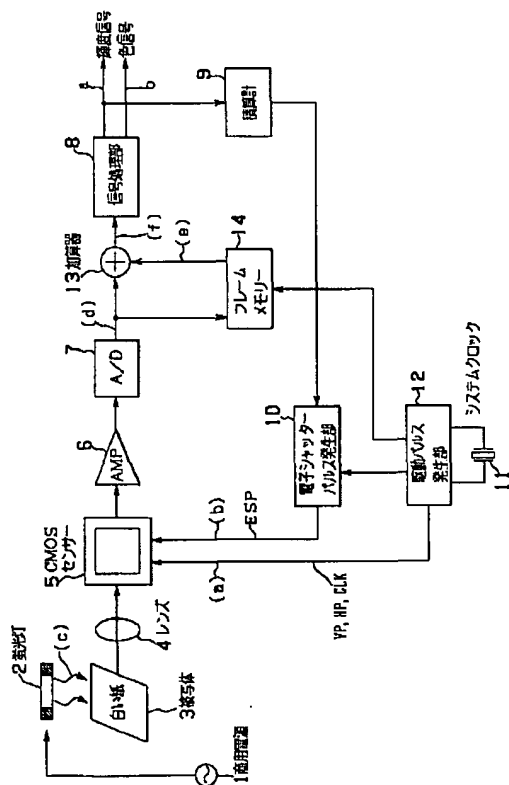
(57) [Abstract]

[Technical problem] The solid state camera which reduced the influence by the flicker is offered.

[Means for Solution] Twice  $(n+1/2)$  {n of the flicker period of a fluorescent lamp 2 sets the read-out period of the photodiode of the CMOS sensor 5 as integer}. Thereby, the phase of the output signal (d) of A/D converter 7 and the output signal (e) of a frame memory 14 shifts 180 degrees (a flicker phase is reversed for every frame), and the output signal (f) of the adder 13 which is the image pick-up signal with which the flicker component for every frame was reduced is obtained by integrating an adder 13 with this signal (d) and signal (e) (addition).

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CLAIMS

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[Claim(s)]

[Claim 1] The solid state image pickup device equipped with the control means which control the light-receiving time of two or more aforementioned optoelectric transducers by the line unit which constitutes the aforementioned line while having two or more optoelectric transducers which are characterized by providing the following, and which were arranged by the matrix two-dimensional and reading an image pck-up signal from two or more of these optoelectric transducers by line sequential through a switch. The light source which irradiates light at the picturized body and from which the quantity of light changes periodically. A storage means to memorize the image pck-up signal read from two or more aforementioned optoelectric transducers by one screen. Next, an addition means to add the image pck-up signal for one screen memorized by the image pck-up signal and the aforementioned storage means for one screen read from two or more aforementioned optoelectric transducers. A means to set it as the period from which the change phase of the change component produced to the aforementioned image pck-up signal at quantity of light change of the aforementioned light source with the light-receiving period of an output means to output the output of this addition means as an image pck-up signal, and two or more aforementioned optoelectric transducers becomes reverse in the signal for one adjoining screen.

[Claim 2] The solid state image pickup device equipped with the control means which control the light-receiving time of two or more aforementioned optoelectric transducers by the line unit which constitutes the aforementioned line while having two or more optoelectric transducers which are characterized by providing the following, and which were arranged by the matrix two-dimensional and reading an image pck-up signal from two or more of these optoelectric transducers by line sequential through a switch. The light source which irradiates light at the picturized body and from which the quantity of light changes periodically. A storage means to memorize the image pck-up signal read from two or more aforementioned optoelectric transducers by one screen. Next, an addition means to add the image pck-up signal for one screen memorized by the image pck-up signal and the aforementioned storage means for one screen read from two or more aforementioned optoelectric transducers. An output means to output the output of this addition means as an image pck-up signal, and a means to set up the light-receiving period of two or more aforementioned optoelectric transducers the twice  $(n+1/2)$  (for n to be an integer) of the period of quantity of light change of the aforementioned light source.

[Claim 3] The solid state camera according to claim 1 or 2 characterized by providing an amplification means to amplify the output of two or more

aforementioned optoelectric transducers, and an analog-to-digital-conversion means to change the output of this amplification means into a digital signal, and to output to the aforementioned storage means.

[Claim 4] Two or more aforementioned optoelectric transducers are solid state cameras according to claim 1 or 2 characterized by providing an accumulation means for the charge by which consisted of photo diodes and photo electric translation was carried out by this photo diode to be supplied per [ aforementioned ] line through a switch, and to accumulate, and the means which reads the charge accumulated at this accumulation means one by one through a switch, respectively.

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**DETAILED DESCRIPTION**

[Detailed Description of the Invention]

[0001]

[The technical field to which invention belongs] this invention relates to the solid state camera using CMOS image sensors as a solid state image pickup device used for the camera for personal computers, an electronic still camera, etc.

[0002]

[Description of the Prior Art] Conventionally, the image pick-up tube has been used

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a        a e a    t s the s -called continuous analog signal, and between each horizontal information which adjoined, the image information accumulated at the photoconduction layer of an image pick-up tube was saved with structure which lessens leakage as much as possible, and was taken out as a continuous ringing by the horizontal continuation scan of an electron beam so that this may not consider the pixels of a picture one by one.

[0003] However, since the solid state image pickup device represented by CCD (Charge Coupled Device = charge-coupled device) was developed, by except [ the object for broadcasting stations, or for particular application ], an image pick-up tube will not be used, and most has put it on a solid state image pickup device, and it has been replaced with.

[0004] What each pixel is memorized [ in the case of the solid state image pickup device ] in the form where it became independent clearly unlike the aforementioned image pick-up tube, and is equivalent to the electron beam scan of an image pick-up tube is a pulse train which becomes the criteria for read-out called clock. And each pixel information is stored as a signal charge, by the clock pulse, it is transmitted one by one, and it is being begun to read it, it is put in order, and serves as a television signal.

[0005] On the other hand, development manufacture of the CMOS image sensors is carried out as a solid state image pickup device which changes to CCD in recent years. these CMOS image sensors (only henceforth a CMOS sensor) -- LSI memory and a processor -- the same -- it is produced by the CMOS process For this reason, it operates by the single power supply and operates by the super-low power (about 1/10) compared with a CCD image sensor. Furthermore, the image pck-up section and an element drive circuit can be accumulated on one chip, and it has the outstanding feature that a high-density highly minute pixel can be constituted.

[0006] Drawing 3 is the block diagram showing the example of composition of the conventional solid state camera which used the CMOS sensor as a solid state image pickup device.

[0007] In drawing 3 , the fluorescent lamp 2 with which power was supplied from the source power supply 1 is illuminating the photographic subject 3 of a solid state camera. Here, it has a uniform reflection factor by crossing to the convenience top of the below-mentioned explanation, and the whole surface, for example, as for the aforementioned photographic subject 3, white paper is chosen.

[0008] Moreover, the lens



pulse based on the perpendicular read-out start signal from the driving pulse generating section 12, and the timing is determined by the aforementioned electronic shutter pulse generating section 10 based on the light-and-darkness information on the picture supplied from an integrator 9 based on the luminance signal a from the signal-processing section 8 (adjustment). That is, from the CMOS sensor 5, control (adjustment) of the shutter speed of an electronic shutter is performed by the electronic shutter pulse generating section 10 so that the signal (image pick-up signal) of the luminosity of a constant rate may be acquired.

[0013] Next, operation of this CMOS sensor 5 is explained in detail, referring to aforementioned drawing 4 .

[0014] In drawing 4 , the photodiode 23 is connected to the MOS switch 24 and the signal read-out switch 25 of charge \*\*\*\*\*, respectively.

[0015] The perpendicular shift register 20 is cleared by the ESP pulse, and the pulse which drives the switch 24 one by one is perpendicularly outputted for every 1 level line of a photodiode 23 by driving by HP pulse. The pulse which sets the switch 24 of the 1st line to ON by HP pulse of the beginning after an ESP pulse is outputted, the cathode of the photodiode 23 of the 1st line is connected to a reference potential (grounding potential) point by it, and the charge accumulated at the photodiode 23 is swept out. The switch 24 of the 2nd line is turned ON by the following HP pulse, it becomes off [ the switch 24 of the 1st line ], and a photodiode 23 accumulates a charge. If the perpendicular shift register 20 is carried out in this way and the charge of all the photodiodes 23 is swept out, an ESP pulse will be again added after 1 perpendicular period, it will return to early operating state, and will repeat it below.

[0016] The perpendicular shift register 21 is cleared by VP pulse, and outputs perpendicularly the pulse which drives the switch 25 one by one for every 1 level line of a photodiode 23 by driving by HP pulse. The pulse which sets the switch 25 of the 1st line to ON by HP pulse of the beginning after VP pulse is outputted, and the stored charge of the photodiode 23 of the 1st line is moved to a capacitor 26 by it, respectively. Simultaneously, the level shift register 22 is cleared by HP pulse, and since it drives so that the pulse which makes a switch 27 turn on one by one horizontally with Clock CLK may be outputted, the charge of a capacitor 26 is serially read to the IV converter 28. The perpendicular shift register 21 outputs the pulse which turns ON the switch 25 of the 2nd line, and the charge of a photodiode 23 is moved to a capacitor 26, and it is read by the following HP pulse with the level shift register 22. If the operation is performed during 1 perpendicular period and the charge of all the photodiodes 23 is read, VP pulse will be impressed again and it will become the recurrence henceforth.

[0017] In here, the charge moved to a capacitor 26 is understood that control of shutter speed is possible by being proportional to a period after an ESP pulse is added until VP pulse is added, and controlling the time interval between an ESP pulse and VP pulse. In addition, since the perpendicular shift registers 20 and 21 drive by HP pulse, the charge-storage period of a photodiode 23 serves as an integral multiple of HP pulse period in fact.

[0018] The relations of the output signal out of input light and the CMOS sensor 5 are indicated to be VP pulse and an ESP pulse to drawing 5 . In addition, in drawing 5 , the system cloc

#####!↑%>♣S>♣drawing 4 is set up by 3 times the flicker period of a fluorescent lamp 2, and the case of a high-speed shutter with the pulse of ESP near [ the shutter speed of a CMOS sensor ] the pulse of VP is shown.  
[0019] By the way, as for the CMOS sensor as the above-mentioned solid state image

pickup device, unlike CCD, the exposure timing of the direction of V between each pixel differs. That is, as shown in aforementioned drawing 4, the stored charge of each aforementioned photodiode 23 is read per line by the shift registers 20 and 21 controlled by the aforementioned ESP pulse and VP pulse (shutter speed determined by time difference s) (held by each aforementioned capacitor 26), and the scan of the output of a CMOS sensor is carried out in the direction of H by the shift register 22, and it is taken out as a signal (the same exposure timing) of 1 H parts. Moreover, the signal for a number (all pixels) (drawing 640x480 pieces) of all the photodiodes 23 is taken out by carrying this out repeatedly several minutes (drawing 480 pieces) of the photodiode 23 arranged in the direction of V (the exposure timing of the direction of V differs).

[0020] For this reason, when a photograph is taken under an indoor fluorescent lamp, a fluorescent lamp flicker generates a light exposure difference in the direction of V which is each pixel of a CMOS sensor, for example. Thereby, the problem that a brightness difference will arise perpendicularly occurs depending on the value of an electronic shutter.

[0021]

[Problem(s) to be Solved by the Invention] Like the above, it was the case where the lighting which has flickers, such as the usual fluorescent lamp using the source power supply as lighting of the photographic subject of a solid state camera which used the CMOS sensor as an image pck-up element, was used, and when the quantity of light was controlled using the electronic shutter of a CMOS sensor, there was a problem (fault) that the disk according to the flicker period of the aforementioned lighting occurred in the image output of the aforementioned solid state camera.

[0022] Then, this invention aims at offering the solid state camera which reduced the influence (generating of a disk) by the flicker which lighting generates even on practical use level, even when the photographic subject under the lighting which has a flicker is picturized in view of such a problem.

[0023]

[Means for Solving the Problem] The solid state camera by invention according to claim 1 While having two or more optoelectric transducers arranged by two-dimensional in procession and reading an image pck-up signal from two or more of these optoelectric transducers to it by line sequential through a switch In the solid state image pickup device equipped with the control means which control the light-receiving time of two or more aforementioned optoelectric transducers by the line unit which constitutes the aforementioned line A storage means to memorize the image pck-up signal read from the light source which irradiates light, and from which the quantity of light changes periodically, and two or more aforementioned optoelectric transducers to the picturized body by one screen, Next, an addition means to add the image pck-up signal for one screen memorized by the image pck-up signal and the aforementioned storage means for one screen read from two or more aforementioned optoelectric transducers, The light-receiving period of an output means to output the output of this addition means as an image pck-up signal, and two or more aforementioned optoelectric transducers It is characterized by providing a means to set it as the period from which the change phase of the change component produced to the aforementioned image pck-up signal with quantity of light change of the aforementioned light source becomes reverse in the signal for one adjoining screen.

[0024] According to invention according to claim 1, the light-receiving period of

two or more optoelectric transducers Since it is set as the period from which the change phase of the change component produced to the aforementioned image pck-up signal with quantity of light change of the light source becomes reverse in the signal for one adjoining screen and the signal for the 1 which carries out contiguity aforementioned screen was added The influence the aforementioned CMOS sensor is influenced by the flicker component which a lighting system has is mitigable to practical use level  $(1/2)$ .

[0025] The solid state camera by invention according to claim 2 While having two or more optoelectric transducers arranged by two-dimensional in procession and reading an image pck-up signal from two or more of these optoelectric transducers to it by line sequential through a switch In the solid state image pickup device equipped with the control means which control the light-receiving time of two or more aforementioned optoelectric transducers by the line unit which constitutes the aforementioned line A storage means to memorize the image pck-up signal read from the light source which irradiates light, and from which the quantity of light changes periodically, and two or more aforementioned optoelectric transducers to the picturized body by one screen, Next, an addition means to add the image pck-up signal for one screen memorized by the image pck-up signal and the aforementioned storage means for one screen read from two or more aforementioned optoelectric transducers, It is characterized by providing an output means to output the output of this addition means as an image pck-up signal, and a means to set up the light-receiving period of two or more aforementioned optoelectric transducers the twice  $(n+1/2)$  (for  $n$  to be an integer) of the period of quantity of light change of the aforementioned light source.

[0026] The solid state camera by invention according to claim 3 is characterized by providing an amplification means to amplify the output of two or more aforementioned optoelectric transducers, and an analog-to-digital-conversion means to change the output of this amplification means into a digital signal, and to output to the aforementioned storage means in addition to the composition in a solid state camera according to claim 1 or 2.

[0027] The solid state camera by invention according to claim 4 is characterized by to provide the accumulation means which the charge to which two or more aforementioned optoelectric transducers consisted of photo diodes, respectively, and photo electric translation was carried out by this photo diode is supplied per [ aforementioned ] line through a switch, and accumulates, and the means which reads the charge accumulated at this accumulation means one by one through a switch in a solid state camera according to claim 1 or 2.

[0028] According to invention according to claim 2 to 4, the read-out period of the image pck-up signal from a CMOS sensor Since the image pck-up signal which twice  $(n+1/2)$  { $n$  of the flicker period of a lighting system considered as integer}, and carried out one-frame period delay of the image pck-up signal from the aforementioned C



source power supply 1 is illuminating the photographic subject 3 of a solid state camera. Here, on account of explanation, cross to the whole surface, and have a uniform reflection factor, for example, the aforementioned photographic subject 3 is white paper.

[0031] Furthermore, the solid state camera of this invention in drawing 1 The lens 4 for carrying out image formation of the photographic subject 3 on the CMOS sensor 5, and the CMOS sensor 5 which changes into an electrical signal the image by which image formation was carried out, The system clock 11 which carries out generating supply of various kinds of timing signals for the CMOS sensor 5 changing into an electrical signal (image pck-up signal) the image by which image formation was carried out, the driving pulse generating section 12, and the electronic shutter pulse generating section 10, The amplifier 6 which amplifies the inputted signal, and A/D converter 7 which changes an analog signal into a digital signal, The adder 13 adding the frame memory 14 which carries out one-frame period delay of the image pck-up signal, and the output (image pck-up) signal of a frame memory 14 and the image pck-up signal before delay, The luminance signal of an one-frame period is inputted and it is constituted by the signal-processing section 8 outputted as a video signal with which the inputted signal was divided into the luminance signal and the chrominance signal, and the integrator 9 which supplies the light-and-darkness information on a picture to the aforementioned electronic shutter pulse generating section 10.

[0032] In the solid state camera constituted as mentioned above, the reflected light from a photographic subject 3 passes along a lens 4, and goes into the CMOS sensor 5. After the output of the CMOS sensor 5 is amplified with amplifier 6, it is changed into a digital signal by A/D converter 7, and is inputted into an adder 13 and a frame memory 14. In a frame memory 14, it drives by the synchronization pulse from the aforementioned driving pulse generating section 12, it operates so that one frame may be delayed at any time to an image pck-up signal, and the delayed image pck-up signal is outputted to an adder 13. It is inputted into a digital disposal circuit 8, and separates into a luminance signal a and a chrominance signal b, and the output of an adder 13 turns into an output of a camera block, and is supplied to interface circuitries, such as a personal computer which is not illustrated.

[0033] Moreover, the pulse supplied to the CMOS sensor 5 has the pulse VP which determines a vertical signal read-out starting position, the pulse HP which determines a horizontal signal read-out starting position, the pulse CLK which decides on the time of level read-out, and the pulse ESP which determines the value of an electronic shutter. Among these, an ESP pulse is generated from the electronic shutter pulse generating section 10, and VP, HP, and a CLK pulse are generated from the driving pulse generating section 12. The driving pulse generating section 12 is dividing-created in each pulse based on the system clock 11 from a system clock 11.

[0034] Furthermore, the electronic shutter pulse generating section 10 creates an ESP pulse based on the perpendicular read-out start signal from the driving pulse generating section 12, and for example, the timing is supplied from an integrator 9 based on the luminance signal a from the signal-processing section 8, it is determined by the aforementioned electronic shutter pulse generating section 10 based on the light-and-darkness information on the picture for one frame (feedback data of the average quantity of light) (adjustment). Control (adjustment) of the shutter speed of an electronic shutter is performed by this [ 10 ], i.e., the

electronic shutter pulse generating section, so that the signal of the luminosity of a constant rate may always be acquired.

[0035] Moreover, the aforementioned system clock 11 is set up for twice  $(n+1/2)$  [ $n$  of the flicker period of a fluorescent lamp 2 so that the read-out period of the photodiode of the CMOS sensor 5 may become integer]. The image pck-up signal output by which generating of the disk by the flicker was sharply mitigated by this also in the image pck-up signal output, i.e., the photography under a fluorescent lamp, as shown in drawing 2 for example, at the time of a high-speed shutter is obtained. This is explained referring to aforementioned drawing 1 and drawing 2.

[0036] Drawing 2 is drawing showing each output signal of the solid state camera in this invention. Setting to drawing 2, the signal (a) and the signal (b) show VP pulse and the ESP pulse at the time of a high-speed shutter, and the signal (c) shows the input signal (image pck-up signal) from the photographic subject 3 with which the fluorescent lamp lighting which has the flicker by which the electric power supply was carried out from the source power supply 1 was irradiated. In addition, with the gestalt of operation of this invention, the read-out period (exposure period) of the photodiode of the CMOS sensor 5 is set up by 3.5 times the flicker period of a fluorescent lamp 2 so that clearly from drawing 2 (c).

[0037] At this time, from A/D converter 7, the signal shown in drawing 2 (d) is outputted, and this signal (d) is supplied to a frame memory 14 and an adder 13, respectively. On the other hand, from a frame memory 14, the signal (e) by which one-frame period delay was carried out in the aforementioned signal (d) is supplied to the adder 13, and addition of these two signals (d) and a signal (e) is performed by the adder 13.

[0038] By the way, since the read-out period of the photodiode of the CMOS sensor 5 is set up by 3.5 times the flicker period of a fluorescent lamp 2 with the gestalt of this operation as stated above, the signal (d) and the signal (e) are in the state where the phase shifted 180 degrees (correctly 1260 degrees). For this reason, after the flicker phase has been reversed for every frame with the adder 13, the aforementioned signal (d) and a signal (e) find the integral (addition). Thereby, the output signal of an adder 13 becomes possible [mitigating a next door and the flicker component for every frame to practical use level  $(1/2)$ , as shown in drawing 2 (f)].

[

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[Effect of the Invention] Also in the photography under the lighting which was described above and which has flickers, such as a fluorescent lamp, according to [ like ] this invention, generating of a disk which is the influence by the flicker which the aforementioned lighting generates can be suppressed as much as possible, and it can decrease to practical use within the limits.

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## DESCRIPTION OF DRAWINGS

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[Brief Description of the Drawings]

[Drawing 1] It is the block diagram showing the gestalt of operation of the solid state camera of this invention using the CMOS sensor as a solid state image pickup device.

[Drawing 2] It is drawing showing each output signal of the solid state camera in this invention.

[Drawing 3] It is the block diagram showing the example of composition of the conventional solid state camera using the CMOS sensor as a solid state image pickup device.

[Drawing 4] It is drawing having shown the internal configuration of the CMOS sensor 5.

[Drawing 5] It is drawing showing each output signal in the conventional solid state camera.

[Description of Notations]

- 1 -- Source Power Supply
- 2 -- Fluorescent Lamp
- 3 -- Photographic Subject
- 4 -- Lens
- 5 -- CMOS Image Sensors
- 6 -- Amplifier (AMP)
- 7 -- A/D Converter
- 8 -- Signal-Processing Section
- 9 -- Integrator
- 10 -- Electronic shutter pulse generating section
- 11 -- System clock
- 12 -- Driving pulse generating section
- 13 -- Adder
- 14 -- Frame memory

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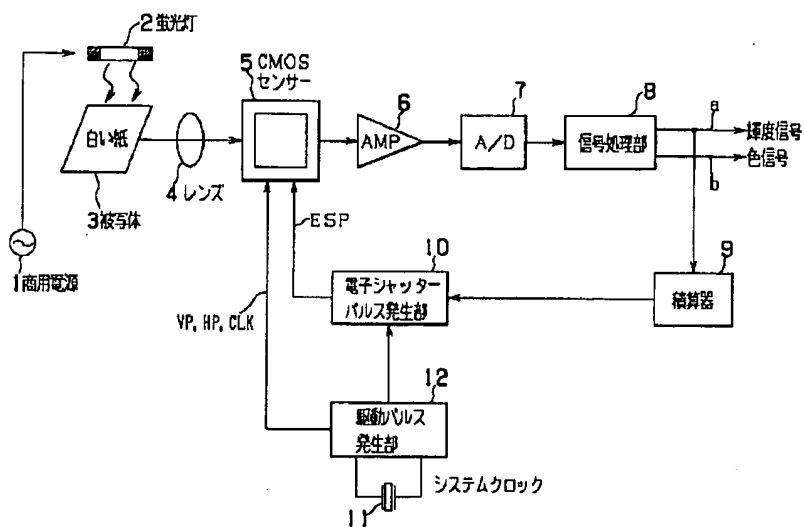
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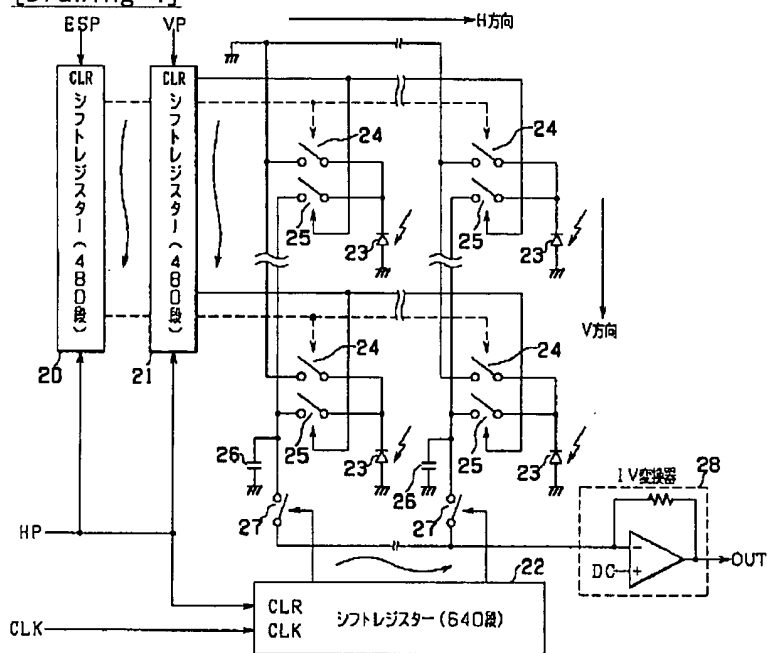
## DRAWINGS

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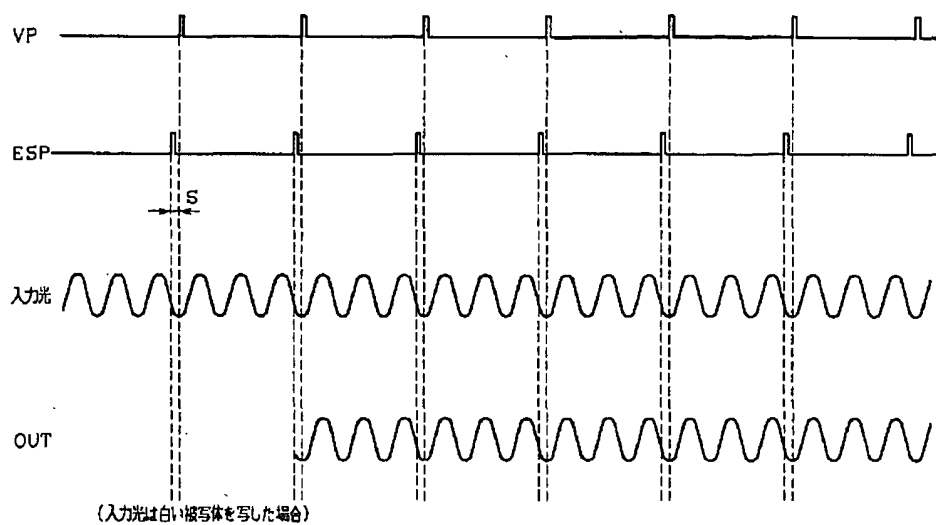




[Drawing 4]



[Drawing 5]



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[Translation done.]